

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:

**RENGAN ET AL.**

Serial No.: 09/904,622

Filed: 13 JULY 2001

For: **DISPLAY PRIVACY FOR  
ENHANCED PRESENTATIONS WITH  
REAL-TIME UPDATES**

Attorney Docket No.: **RPS920010005US1**

Confirmation No.: **2989**

Examiner: **NGUYEN, K.**

Art Unit: **2629**

**REPLY BRIEF**

MS Appeal Brief-Patents  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

This Reply Brief is submitted in response to the Examiner's Answer dated July 21, 2006.

## REMARKS

On page 7 of the Examiner's Answer, the Examiner asserts that in col. 17, lines 45-54, *Chee* teaches information being held in the first memory location, and the information will then be transferred and changed into the second memory. Col. 17, lines 45-54 of *Chee* explain

However, the display FIFO's 56 and 56' will be allowed sufficient access to the DRAM 38 that the FIFO's do not run out of display data originating with the particular memory spaces 100' and 102'. Accordingly, although the accesses to the DRAM 38 are intermittent for each of the display FIFO's 56 and 56', the displays 14/24 and 14/24' will each be supplied simultaneously with different display data. That is, the user of the computer system 10 will see a different image presented on the displays 14 and 24 simultaneously.

It is not clear which two of *Chee*'s memories the Examiner considers as the first and second memory locations, but it is clear that the above-cited passage does not teach or suggest the holding of information in a first memory location (or specifically the claimed retaining step).

On pages 7-8 of the Examiner's Answer, the Examiner states that *Chee* discloses a system having two memory locations along with two FIFOs for displaying different images on two different displays, but *Chee* does not disclose a concurrent display mode for displaying identical images on two different displays. Appellants agree. The Examiner continues to state that *Ranganathan* discloses a system having a concurrent display mode for displaying identical images on two different displays. Appellants also agree. However, since *Ranganathan*'s method of displaying utilizes a single memory location, hence, only the same image can be displayed regardless of how many displays *Ranganathan* intended to use. Since the Examiner did not provide any explanation, it is unclear as to how *Ranganathan*'s method of displaying that uses a single memory location can be applied to *Chee*'s two memory locations implementation. For example, it is unclear whether *Ranganathan*'s teaching of the single memory location should be applied to *Chee*'s memory location 100' or memory location 102'.

If the Examiner's intention is to simply add *Ranganathan*'s concept of concurrent display mode to *Chee*'s concept of split display mode for the purpose of rendering the claimed invention

obvious under § 103 rejection without providing any motivation or suggestion along with how the above-mentioned teachings can be combined, the Examiner does not meet the criteria for establishing a *prima facie* case of obviousness under MPEP § 2143.

For the reasons stated above, Appellants believe the § 103 rejection for Claims 1-7 and 24-37 is improper and should be reversed.

No fee or extension of time is believed to be necessary; however, in the event an additional fee or extension of time is required, please charge that fee or extension of time requested to the Lenovo Deposit Account **50-3533**.

Respectfully submitted,



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